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| 10/066,849 | 02/04/2002 | Sung-Kwon Lee | 29926/38060 | 5173 |

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| EXAMINER | |
|---|---|
| RUGGLES, JOHN S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 1756 | |

DATE MAILED: 02/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/066,849 | LEE ET AL. |
| | Examiner | Art Unit |
| | John Ruggles | 1756 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2 and 4-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-14* is/are rejected.

7)☒ Claim(s) *1,2 and 4-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 3 and 15-20 have now been cancelled and claims 1-2, 6-8, and 9-12 have been currently amended. Therefore, only claims 1-2 and 4-14 remain under consideration.

### *Drawings*

The previous objection to Figure 3D has been overcome by amendments to the description thereof in the specification.

### *Specification*

While the abstract of the disclosure has been amended to obviate most of the previous objections, it is again objected to because the currently added phrase "and second interlayer insulating layer" in lines 5-6 should have been --and the first etching stop layer-- 34 in order to correspond to Figure 3B as described at page 6, lines 5-7 of the original specification. Additionally, the amended version of the abstract has now been lengthened to over 150 words. The first 2 lines should be shortened and simplified by changing "Disclosed is a method for manufacturing multi-level interconnections using a dual damascene process. The method includes: " to --Dual damascene manufacturing of multi-level interconnections that includes: --. Correction is required. See MPEP § 608.01(b).

While amendments to the specification have overcome most of the previous exemplified objections thereto, examples of those remaining and/or introduced by current amendments to the specification are set forth below.

35 U.S.C. 112, first paragraph, requires the specification to be written in "full, clear, concise, and exact terms." The specification is still replete with terms, which are not clear, concise and exact. The specification should again be revised carefully in order to comply with 35 U.S.C. 112, first paragraph. Examples of some unclear, inexact or verbose terms used in the specification are: (1) in the amendment to the paragraph beginning on page 8, line 19 of the original specification (found at the top of page 3 in the amendment filed 2 January 2004), "and electroless deposition" should be changed back to the original language of --**an** electroless deposition--, to be grammatically correct; (2) at lines 14-15 on page 4 of the original specification, "prevent capacitance value increasing" should be changed to --prevent the capacitance value from increasing--, also to be grammatically correct; (3) at line 32 on page 5 of the original specification, "selectively etched to exposure a part" must be corrected to --selectively etched to expose a part--; and (4) in the amendment to the paragraph beginning on page 9, line 5 of the original specification (also found on page 3 of the amendment), "Since the minimum etching stop layer...a margin of a trench etching process may be maximized" is still confusing and does not clearly and concisely set forth the purpose for applicants' invention as supported by the original disclosure, even though this currently amended version is an improvement over the original language. Applicants are also requested to specify where support for these changes can be found in the originally filed specification. Applicants are again reminded that due to the number of errors, those listed here are merely *examples* of the corrections needed and do *not* represent an exhaustive list thereof.

Appropriate correction is required. A statement that it contains no new matter must accompany an amendment filed making all appropriate corrections.

***Claim Objections***

While amendments have overcome most of the previous objections to the claims, those still remaining are set forth below, along with new objections necessitated by these amendments.

Claims 1-2 and 4-14 are now objected to because of the following informalities: (1) in lines 4-5 of currently amended claim 1 on page 4 of the amendment, "a first interlayer insulating layer of disposed on" (emphasis added) must be changed to --a first interlayer insulating layer disposed on--, to be grammatically correct and in lines 15-16 of currently amended claim 1, "etching stop patterns" should now be changed back to the original language phrase --etching stop pattern--, in order to be consistent with this phrase as currently amended in line 13 of claim 1; (2) in line 6 of currently amended claim 2 on page 4 of the amendment, "the etching stop patterns are formed" should now be changed to --the etching stop pattern is formed--, in order to be consistent with this phrase as currently amended in line 13 of claim 1; (3) in line 2 of claim 4, "etching stop patterns" should now be changed to --etching stop pattern--, also to be consistent; and (4) in line 4 of currently amended claim 7 on page 5 of the amendment, "plasma enhanced chemical vapor deposition method" should be corrected to --plasma enhanced chemical vapor deposition--, in order to be grammatically correct (as an alternative to subsequently recited "low pressure chemical vapor deposition" found in lines 4-5 of this currently amended claim 7). Claims 2 and 4-14 are dependent on claim 1. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

While current amendments to the claims have overcome the previous rejection of claims 1-14 under the second paragraph of 35 U.S.C. 112, another new rejection under this section has been necessitated by amendment and is set forth below.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14 are still rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Currently amended claim 1 is still not fully clear when compared to the original specification with regard to just which layers are formed directly underneath and in contact with the third interlayer insulating layer 36. While lines 6-7 of amended claim 1 recite "forming a third interlayer insulating layer on the first interconnection line and the second interlayer insulating layer", Figure 3B clearly shows that the third interlayer insulating layer 36 is formed directly over the first interconnection line 35 and the first etching stop layer 34 (emphasis added), as described at lines 5-7 on page 6. The first etching stop layer 34 was previously formed over the second interlayer insulating layer 33, as described at lines 27-30 on page 5 of the original specification in reference to Figure 3A. Therefore, this recitation in amended claim 1 has been interpreted to read --forming a third interlayer insulating layer on the first interconnection line and the first etching stop layer--. However, applicants must still amend claim 1 accordingly in order to correlate with the instant figures and their corresponding written descriptions, as originally filed. Claims 2 and 4-14 are dependent on claim 1.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-5, and 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (US Patent 6,093,632) in view of Lin, et al. (US Patent 6,042,999).

Lin '632 teaches a modified dual damascene method for manufacturing multi-level interconnection lines in a semiconductor device. The method involves forming conductive (copper, Cu, instant claim 13) interconnection lines 2 in a first (1st) insulator (silicon oxide) 1, which is understood to be on a semiconductor substrate. Layers 1 and 2 are covered by a 1st etching stop layer 3 (silicon nitride, instant claim 3), a second (2nd) insulator (silicon oxide) 4 formed by either plasma enhanced chemical vapor deposition (PECVD) or low pressure chemical vapor deposition (LPCVD) to 4,000-15,000 Å thick (column 4, lines 6-9, instant claims 9-10), and a 2nd etching stop layer 10a (silicon nitride 200-2,000 Å thick by e.g., PECVD, etc., column 5, lines 25-27, instant claims 11-12), as shown in Figure 4 (column 5, lines 18-28). A resist pattern 11 is used as an etching mask to pattern narrow openings 12a for via holes in the 2nd etching stop layer 10a, to form a patterned etching stop layer 10b, as shown in Figure 5 (column 5, lines 29-43). After removing the resist, the patterned etching stop layer 10b is covered by a third (3rd) insulator layer 13 (silicon oxide by e.g. PECVD, etc. to about 3,000-

15,000 Å thick), followed by forming another patterned resist mask 14, having wider openings 15a for forming wide trenches connecting over the narrow via holes, as shown in Figure 6 (column 5, lines 43-53, instant claim 5). The wide trenches and narrow via holes are etched through the resist mask 14 and etching stop pattern portions 10b through the insulators 13 and 4 and etching stop layers 10b and 3 down to the conductive interconnection lines 2, as shown in Figure 7 (column 5, line 54 to column 6, line 8, instant claim 4). A conductive layer 16 is formed to fill the trenches and connected underlying via holes onto the tops of conductive lines 2, as shown in Figure 8 (column 6, lines 9-29, instant claims 1-2). While not specifying the thickness of the Cu conductive interconnection lines 2, the figures suggest this thickness is similar to those of insulator layers 3 and 13 (or about 3,000-15,000 Å thick, instant claim 14). Lin '632 patterns the etching stop layer to leave only small area islands 10b, in order to reduce or limit increase in capacitance usually caused by wider area etching stop layers (column 2, lines 15-25). Also, while the teachings of Lin '632 are described in terms of this method as a preferred embodiment, it is understood by those skilled in the art of dual damascene multi-level interconnection manufacture of semiconductor devices that various changes may be made in the details of this embodiment without departing from the spirit and scope of these teachings (column 6, lines 36-40).

While teaching a dual damascene method for manufacturing multi-level interconnection lines similar to the instant invention, Lin '632 does not specify forming the via holes before forming the patterned etching stop patterns around the via inlets and subsequent trench patterning of the overlying 3rd insulator layer.

Lin '999 shows a robust dual damascene method of manufacturing multi-level interconnection lines in a semiconductor device that involves formation of a via 145, before forming an overlying trench 165, as shown in Figures 2b and 2f (column 5, line 20 to column 6, line 18).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have changed the order of steps in the embodiment described by Lin '632 so as to form via openings before forming the patterned etching stop layer portions 10b, then overlying and patterning the 3rd insulator layer to form trenches therein. This is because Lin'632 suggests changes to the details of his preferred embodiment without departing from the spirit and scope of those teachings relating to use of patterned reduced area islands of etching stop material to reduce capacitance under that which would have resulted if a wider area etching stop layer had been used. Also, formation of via holes followed by subsequent formation of trenches over these via holes (via first, rather than trench first) is already known in dual damascene semiconductor device manufacture, as shown by Lin '999.

Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin '632 in view of Lin '999 and further in view of Huang (US Patent 6,268,283).

While teaching other aspects of the instant invention, neither Lin '632 nor Lin '999 specifically teaches forming a void within the via hole by covering it with an overlying insulating layer.

Huang describes a dual damascene method for manufacturing multi-level interconnects in a semiconductor device (column 1, lines 1-11). The method includes etching through a patterned

resist 212 to form a via hole 214 through a hard mask 210, a dielectric 208, and etching stop layers 206 and 204 down to an interconnecting conductor 202, as shown in Figure 2B (column 3, lines 29-32). After removing remaining resist 212, a cap layer 216 is formed over the hard mask 210, covering the top region 218 of via hole 214 and leaving a void in the lower region of the via hole 214, as shown in Figure 2C (instant claim 6). The cap layer 216 (e.g., silicon oxide, silicon nitride, silicon oxynitride, etc., preferably formed by PECVD to a thickness of 1,000-2,000 Å, instant claims 7-8) supports a subsequent overlying resist having a trench pattern 224 and also prevents low-level devices or layers (e.g., dielectric layers 208 and 204, etc.) from being damaged during developing of the resist (column 3, lines 33-56). The cap layer 216, the hard mask 210, and the dielectric 208 are then etched using the patterned resist 224 as an etching mask to form a trench 226, as shown in Figure 2D (column 3, lines 57-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have used a cap layer to form a void within the via hole as described by Huang in the dual damascene method taught by Lin '632 and shown by Lin '999 in order to support an overlying resist pattern and protect lower-level devices and layers as described by Huang and also because all three references relate to the same art of dual damascene manufacture of multi-level interconnects in semiconductor devices.

### *Response to Arguments*

Applicant's arguments filed 2 January 2004 have been fully considered but they are not deemed persuasive.

The previous objection to Figure 3D has been overcome by amendments to the description thereof in the specification.

While the abstract of the disclosure has been amended to obviate most of the previous objections, it has again been objected to for the reasons set forth above.

While amendments to the specification have overcome most of the previous exemplified objections thereto, examples of those remaining and/or introduced by current amendments to the specification have been set forth above.

While amendments have overcome most of the previous objections to the claims, those still remaining have been set forth above, along with new objections necessitated by these amendments.

While current amendments to the claims have overcome the previous rejection of claims 1-14 under the second paragraph of 35 U.S.C. 112, another new rejection under this section has been set forth above, as necessitated by amendment.

In response to applicant's arguments against the references individually (e.g., Lin '632 at the bottom of page 9, etc.), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). While Lin '632 teaches etching through the 2nd etching stop layer 10b along with the overlying insulator 13 during the trench formation shown in Figure 7, the via hole 12b has been previously etched with a narrower width in accordance with the via hole opening 12a defined by the 2nd etching stop layer pattern 10b in Figure 6 (before the trench formation). Etching stop layers are primarily used to protect portions of an underlying layer during etching of an

overlying layer. These etching stop layers are known in the art to sometimes be etched through along with an overlying layer, but still serve the intended purpose as long as the etching is stopped before undesirable etching occurs in the underlying layer. So, Lin '632 still uses the patterned 2nd etching stop layer 10b surrounding the intended via hole region 12a to protect the underlying insulator 4 from undesirable etching. Furthermore, the additional reduction in width of the remaining pattern of residual 2nd etching stop layer taught by Lin '632 would be expected to result in even further reduction of undesirable capacitance, which is the same result sought by the instant invention. Therefore, the instant invention is not distinguished over this prior art of record simply based on a greater proportion of the 2nd etching stop layer remaining in the dual damascene structure.

While Lin '632 does not specify forming the via holes before forming the patterned etching stop patterns around the via inlets and subsequent trench patterning of the overlying 3rd insulator layer, Lin '999 has been cited to show that formation of via holes followed by subsequent formation of trenches over these via holes (via first, rather than trench first) was already known in dual damascene semiconductor manufacture. Thus, the previous rejection of claims 1-2, 4-5, and 9-14 in view of the ***combination*** of these references has been maintained.

Applicants suggest on page 10 of the amendment that Huang's use of a cap layer to create a void in the via hole during a dual damascene process in order to support an overlying resist pattern and protect lower-level devices and layers (e.g., dielectric layers 208 and 204, etc.) is not combinable with Lin '632 and Lin '999 to achieve the same result as that of the instant invention. Applicants assert that this is because the instant invention includes selective etching of the 4th interlayer insulating layer, which acts as a cap layer to create a void in the via hole. However,

Huang's cap layer 216 (e.g., silicon oxide, silicon nitride, silicon oxynitride, etc., preferably formed by PECVD to a thickness of 1,000-2,000 Å) supports a subsequent overlying resist having a trench pattern 224 and also prevents low-level devices or layers from being damaged during developing of the resist (column 3, lines 33-56). The cap layer 216, the hard mask 210, and the dielectric 208 are then etched using the patterned resist 224 as an etching mask to form a trench 226, as shown in Figure 2D (column 3, lines 57-67). Therefore, instant claims 6-8 are still believed to be obvious over the same cited prior art of record (Lin '632, Lin '999, and Huang) as previously set forth. Accordingly, the previous rejection of these claims has also been maintained.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Ruggles whose telephone number is 571-272-1390. The examiner can normally be reached on Monday-Thursday and alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John Ruggles
Examiner
Art Unit 1756

MARK F HUFF
SUPERVISORY PATENT EXAMINER
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